Avi Patel

US Citizen | avipate415@gmail.com | (848)-667-9328 | linkedin.com/in/avipatelengineering | github.com/Avi-Patel-1 | avipatelportfolio.com

EDUCATION

Clemson University — Clemson, SC
Master of Science in Computer Engineering — Expected May 2028; GPA 4.00/4.00
Bachelor of Science in Computer Engineering — May 2026; GPA 3.62/4.00

EXPERIENCE

Draper — Cambridge, MA
Systems Engineering Co-op — Sep 2026 – Present

- Developing and validating embedded Python/C software on NVIDIA Jetson for an ultra-low-power, real-time stellar guidance system for hypersonic missiles, integrating sensor processing and debugging hardware–software interfaces for reliable navigation.

Siemens — Alpharetta, GA
Technical Consulting Intern — May 2026 – Aug 2026

- Led the redesign of Siemens' U.S. PCS 7 installed-base process, consolidating 700+ customer and site records into a validated workflow designed to scale across additional products and countries.
- Designed the platform with Power Apps, SharePoint, Power Automate, Power Query, and Power BI to automate field-data collection, validation, and reporting; developed AI agents to identify opportunities, estimate revenue, and recommend next actions.
- Built alignment through conversations with engineers, consultants, sales leaders, customers, and headquarters stakeholders; applying the platform at a customer visit surfaced $300K+ in modernization potential and generated interest in broader adoption.

Cadence Design Systems — San Jose, CA
ASIC Physical Design Intern — May 2025 – Aug 2025

- Implemented two ASIC blocks, including a Tensilica HiFi3 DSP, from RTL through synthesis, floorplanning, placement, CTS, routing, timing closure, and signoff using Cadence Genus, Innovus, and Tempus; achieved DRC-clean 0 WNS/TNS timing closure at 160 MHz.
- Executed 40+ controlled characterization runs across 50–178.5 MHz targets, floorplans, utilization, CTS settings, and 130 nm HS/NOM/LP libraries; improved implementation QoR by more than 10% while quantifying timing, power, and area tradeoffs.
- Built Tcl, Bash, and Python automation for benchmark sweeps and QoR/timing reporting, reducing recurring flow runtime by approximately 20%.
- Diagnosed DRC/antenna, clock-gating/library, memory-flow, hold, congestion, and timing failures; implemented corrective fixes and presented design reviews and methodology recommendations to senior applications engineers.

HIGHLIGHTED PROJECTS

AI-Powered Fruit Fly Genetics Platform - https://fruitflyai.org

- Architected an end-to-end Physical AI platform for the Clemson Institute of Human Genetics that autonomously captures, transports, classifies, sorts, and phenotypes fruit flies through a complete climbing-assay workflow.
- Developed a cascaded vision pipeline combining YOLOv26 localization with a neural phenotype classifier, achieving 97% accuracy at 89% automated coverage after training on NVIDIA H100/A100 GPUs and Clemson's Palmetto supercomputer.
- Deployed real-time edge inference on a Raspberry Pi 5 and engineered closed-loop vision-to-actuation control for precision motion, vibration, and solenoid-vacuum handling; designed a custom PCB using KiCad.
- Won 1st Place at Clemson's 2026 Senior Design Expo, with follow-on research progressing toward publication and patent protection for derivative designs.

Autonomous Bowling Robot - https://bowlingrobot.com

- Built an autonomous 10-pin bowling robot using Python, MATLAB, and Simulink, integrating camera-based sensing, image processing, motor control, servo actuation, and rack-and-pinion hardware into a real-time mechatronic system.

Verilog FPGA Multi-Mode Timing Controller

- Led a three-person team in designing a synthesizable Verilog controller with real-time clock, alarms, stopwatch, countdown, snooze, PWM audio, debouncing, and multiplexed display functions.
- Built ModelSim testbenches for rollover behavior, mode transitions, and concurrent timing functions, then validated the design on FPGA hardware.

SKILLS

ASIC & Physical Design: Cadence Genus/Innovus/Tempus; RTL-to-GDSII, synthesis, floorplanning, place-and-route, CTS, STA/MMMC/SDC, timing closure, DRC/antenna/hold debugging, PPA/QoR
FPGA & Embedded Systems: Verilog/SystemVerilog, Vivado/Vitis HLS, Quartus Prime, ModelSim, PYNQ-Z2, STM32, NVIDIA Jetson, Raspberry Pi, Arduino; RTL design/verification, AXI interfaces, sensor interfacing, motor control
PCB & Circuit Design: Altium, KiCad, Cadence Allegro/Virtuoso, LTspice; schematic design, PCB layout, board bring-up
Lab & Prototyping: Oscilloscopes, digital multimeters, function generators, bench power supplies, soldering, circuit debugging; SolidWorks, Fusion 360, 3D printing
Software & Controls: C/C++, Python, Tcl, Bash, Perl, MATLAB/Simulink, Linux, Git, GDB, NumPy/Pandas